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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,103	SMITH ET AL.	
	Examiner	Art Unit	
	JONATHAN R. PLANTE	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,10-13 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,10-13 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Applicant's communication filed 02/09/2009 in response to PTO Office Action mailed 12/05/2008. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/09/2009 has been entered.

Claim Amendments

3. Acknowledgment of receiving amendments to the claims, which were received by the Office on 02/09/2009. Claims 8 and 10-13 are amended, claims 1-7, 9, and 14-15 are canceled, and claims 16-22 are new.

Response to Arguments

4. Applicant's arguments with respect to claims 8, 10-13, and 16-22 have been considered but are moot in view of the new ground(s) of rejection.

New Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 8, 10-11, 13, and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Akkerman (US 2004/0225977 A1 November 11, 2004)**

(Claim 8): Akkerman discloses:

a. Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, **["A system and method for simulating clock drift between asynchronous clock domains. In one embodiment, a first circuit portion is positioned in a first clock domain to transmit a first data sequence. An intermediate circuit portion receives the first data sequence and, responsive to a control signal, transmits a second data sequence to a second circuit portion positioned in a second clock**

domain. The second data sequence is subjected to drift relative to the first data sequence." (ABSTRACT), SIMULATED DIGITAL DESIGN (Figure 1, 102)] comprising:

b. a first asynchronous clock domain; **["The digital circuit 100 comprises a first integrated circuit domain 104, ICD1, driven by a first clock, CLK1" (Paragraph 0010)]**

c. a second asynchronous clock domain, **["a second integrated circuit domain 106, ICD2, driven by a second clock, CLK2 (Paragraph 0010)]** wherein

d. at least one of the one or more jitter elements **[DELAY REGISTER (Figure 2, 214), MULTIPLEXER (Figure 2, 216), RANDOM SELECTOR (Figure 2, 220)]** is insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain **["To simulate clock drift between the integrated circuit domains 104S and 106S of the simulated digital design system 102, a clock drift simulation circuit 110 is positioned between the first integrated circuit domain 104S and the second integrated circuit domain 106S." (Paragraph 0012), "FIG. 2 illustrates one embodiment of system 200 for simulating clock drift between asynchronous clock domains 202 and 204. As will be discussed in more detail herein below, a clock drift simulation circuit 206 is positioned intermediately to the circuit portion 202 and the circuit portion 204 to simulate clock drift there between." (Paragraph 0013), "Within the clock drift simulation circuit 206, the data path 212 provides**

the data to a delay register 214 and a Multiplexer (MUX) block 216. In one embodiment, the delay register is clocked by the CLK-ICD-RX clock and holds the data provided by the data path 212 for one clock cycle before transmitting the data to the MUX block 216 via data path 218 as indicated by the notation D.sub.REG DATA in FIG. 2." (Paragraph 0014), *Where the clock drift simulation circuit operates according to the clock of the second asynchronous clock domain interpreted as the clock drift simulation circuit is 'in the second asynchronous clock domain at the circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain.'"*]

(Claim 10): In further view of Claim 8, Akkerman discloses:

a. wherein the at least one of the one or more jitter elements comprise one or more delay elements for introducing predetermined timing delays which is randomly exercised **["Within the clock drift simulation circuit 206, the data path 212 provides the data to a delay register 214 and a Multiplexer (MUX) block 216. In one embodiment, the delay register is clocked by the CLK-ICD-RX clock and holds the data provided by the data path 212 for one clock cycle before transmitting the data to the MUX block 216 via data path 218 as indicated by the notation D.sub.REG DATA in FIG. 2." (Paragraph 0014), "The data sequence provided by data path 226, i.e., the data within the clock domain 204, may exhibit clock drift relative to the data sequence**

provided by the data path 208 of the clock domain 202. For example, assuming that the data is one-bit wide, if the control signal 222 comprises "1," then the data provided via data path 212 is forwarded to the clock domain 204. This undelayed data may be considered "fast" data that is representative of a data portion that is not affected by clock drift. If the control signal 222 comprises "0," however, then the data provided by the delay register 214 via data path 218 is selected to be forwarded to the clock domain 204. This data has been delayed by the delay register 214 for one cycle. Hence, depending on the control signal 222, the data sequence provided via data path 208 relative to the data sequence provided via data path 226 may include synchronization abnormalities, such as fast data portions, delayed data portions, duplicate data portions, and absent data portions, for example, that are indicative of clock drift." (Paragraph 0016)]

(Claim 11): In further view of Claim 8, Akkerman discloses:

a. wherein the at least one of the one or more jitter elements comprise x generator elements **[RANDOM SELECTOR (Figure 2, 220)]** for introducing predetermined signal values which are randomly generated **["A random selector 220 generates an N-bit wide control signal 222 which controls MUX block 216. As illustrated, the control signal may be a randomly generated control signal. Depending on the value of the control signal 222, the MUX block 216 selects either the input data provided by data path 212 or the input**

data provided by data path 218 to be forwarded as output to the clock domain 204. Within the clock domain 204, the data is forwarded to register 224 and, via data SENT DATA path 226, the data is forwarded to register 228 before entering the core of the digital logic of clock domain 204. As illustrated, register 224 and register 228 are driven by the CLK-ICD-RX clock signal." (Paragraph 0015)]

(Claim 13): In further view of Claim 8, Akkerman discloses:

a. wherein the at least one of the one or more jitter elements are automatically inserted using predetermined modules **["As previously mentioned, the clock drift simulation circuit 206 may be effectuated as a function modeled by a design synthesis editor in a HDL environment such as a VHDL environment, a Verilog description language environment, or an ABEL environment, for example. In one embodiment, the clock drift simulation circuit may comprise an HDL-compatible module operable to delay data crossing an asynchronous clock boundary. The following code portion may be employed in conjunction with a Verilog synthesis tool to effectuate one embodiment of the system for simulating clock drift between asynchronous clock domains:" (Paragraph 0019)]**

(Claim 16): In further view of Claim 8, Akkerman discloses:

a. wherein the one or more jitter elements are representable as logical elements, **[DELAY REGISTER (Figure 2, 214), MULTIPLEXER (Figure 2, 216)]** the values of which are randomly set **["A random selector 220 generates an N-bit wide control signal 222 which controls MUX block 216. As illustrated, the control signal may be a randomly generated control signal. Depending on the value of the control signal 222, the MUX block 216 selects either the input data provided by data path 212 or the input data provided by data path 218 to be forwarded as output to the clock domain 204. Within the clock domain 204, the data is forwarded to register 224 and, via data SENT DATA path 226, the data is forwarded to register 228 before entering the core of the digital logic of clock domain 204. As illustrated, register 224 and register 228 are driven by the CLK-ICD-RX clock signal." (Paragraph 0015)]**

(Claim 17): In further view of Claim 8, Akkerman discloses:

a. wherein at least one of the one or more jitter elements is configured to jitter data from the first asynchronous clock domain **["Within the first clock domain 202, an N-bit wide data path 208 provides data to a register 210 which is driven by the CLK-ICD-TX clock. It should be appreciated that if the data path is N-bit wide and N>1, then the register 210, and similarly other components of the system 200, will comprise an appropriate arrangement of N-tuple components. For example, when N>1 the clock domain 202**

may comprise N registers 210 to handle the N-bit wide data path. The register 210, in turn, provides the data to the clock drift simulation circuit 206 via data path 212, which is labeled REC DATA in FIG. 2. Within the clock drift simulation circuit 206, the data path 212 provides the data to a delay register 214 and a Multiplexer (MUX) block 216. In one embodiment, the delay register is clocked by the CLK-ICD-RX clock and holds the data provided by the data path 212 for one clock cycle before transmitting the data to the MUX block 216 via data path 218 as indicated by the notation D.sub.REG DATA in FIG. 2." (Paragraph 0014), "A random selector 220 generates an N-bit wide control signal 222 which controls MUX block 216. As illustrated, the control signal may be a randomly generated control signal. Depending on the value of the control signal 222, the MUX block 216 selects either the input data provided by data path 212 or the input data provided by data path 218 to be forwarded as output to the clock domain 204. Within the clock domain 204, the data is forwarded to register 224 and, via data SENT DATA path 226, the data is forwarded to register 228 before entering the core of the digital logic of clock domain 204. As illustrated, register 224 and register 228 are driven by the CLK-ICD-RX clock signal." (Paragraph 0015), "The data sequence provided by data path 226, i.e., the data within the clock domain 204, may exhibit clock drift relative to the data sequence provided by the data path 208 of the clock domain 202. For example, assuming that the data is one-bit wide, if the

control signal 222 comprises "1," then the data provided via data path 212 is forwarded to the clock domain 204. This undelayed data may be considered "fast" data that is representative of a data portion that is not affected by clock drift. If the control signal 222 comprises "0," however, then the data provided by the delay register 214 via data path 218 is selected to be forwarded to the clock domain 204. This data has been delayed by the delay register 214 for one cycle. Hence, depending on the control signal 222, the data sequence provided via data path 208 relative to the data sequence provided via data path 226 may include synchronization abnormalities, such as fast data portions, delayed data portions, duplicate data portions, and absent data portions, for example, that are indicative of clock drift." (Paragraph 0016)]

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 12 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akkerman (US 2004/0225977 A1 November 11, 2004).**

(Claim 12): Akkerman fails to explicitly teach:

a. wherein the jitter elements are interactively inserted by a user

However, Akkerman et al. teaches the application of simulation software using logic code modules to simulate clock drift. It would have been obvious to one skilled in the art that a logic engineer using the simulation software (i.e. VHDL) would be able to insert the clock drift module manually when simulating the asynchronous boundary in order to allow the logic engineer to explicitly test for the condition. The option of allowing a user or software to insert the clock drift simulation module are obvious options to one skilled in the art. The benefit of allowing automatic insertion provides for a comprehensive testing, while allowing the user to insert the module allows for explicitly boundaries to be tested by the user reducing the simulation time by reducing the number of boundaries to be simulated. There an obvious simulation time to simulation coverage relationship to be considered where each option has positive and negative implications.

(Claims 18-22): Are rejected in view of the rejection of Claims 8, 10, 11, 12, and 13 respectively in that Akkerman teaches the simulation of an electronic circuit above and it would have been obvious to one skilled in the art that the simulated circuit could be constructed physically as a real electronic circuit by one skilled in the art where the motivation to construct the physical circuit would be to confirm the simulation results with real world results. Additionally by physically constructing the circuit it would allow one skilled in the art to test the circuit without the need of expensive simulation

hardware/software. The Examiner also notes that Figure 2 depicts an electronic circuit by a network of logical elements.

Conclusion

9. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application. **Failure to show support can result in a non-compliant response.**

When responding to this office action, Applicant is advised that if Applicant traverses an obviousness rejection under 35 U.S.C. 103, a reasoned statement must be included explaining why the Applicant believes the Office has erred substantively as to the factual findings or the conclusion of obviousness See 37 CFR 1.111(b).

Additionally Applicant is further advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571)

272-9780. The examiner can normally be reached on Monday -- Thursday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. R. P./
Examiner, Art Unit 2182
April 7, 2009

/Alan S Chen/
Primary Examiner, Art Unit 2182
April 9, 2009